Am9513 • AmZ8073

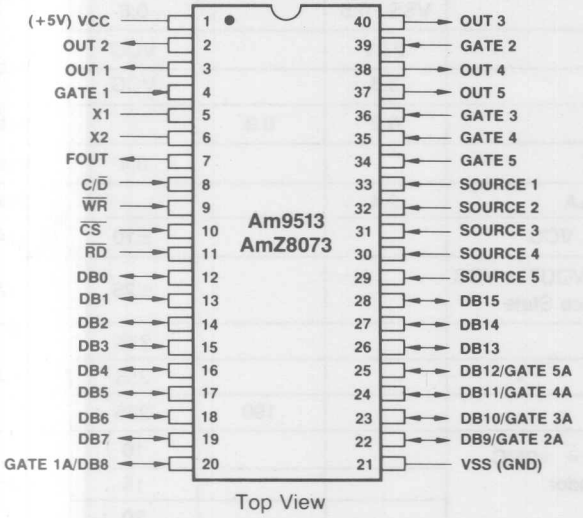
System Timing Controller
Advanced Micro Devices

ELECTRICAL SPECIFICATION

DISTINCTIVE CHARACTERISTICS

- Five independent 16-bit counters
- High speed counting rates
- Up/down and binary/BCD counting
- Internal oscillator frequency source
- Tapped frequency scaler
- Programmable frequency output
- 8-bit or 16-bit bus interface
- Time-of-day option
- Alarm comparators on counters 1 and 2
- Complex duty cycle outputs
- One-shot or continuous outputs
- Programmable count/gate source selection
- Programmable input and output polarities
- Programmable gating functions
- Retriggering capability
- +5 volt power supply
- Standard 40-pin package
- 100% MIL-STD-883 reliability assurance testing

CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

Figure 1.

MMC-088

GENERAL DESCRIPTION

The Am9513 System Timing Controller is an LSI circuit designed to service many types of counting, sequencing and timing applications. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digital one-shots, time-of-day clocking, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watching timing, event count accumulation, waveform analysis and many more. A variety of programmable operating modes and control features allow the Am9513 to be personalized for particular applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-high or active-low input polarity. Both hardware and software gating of each counter is available. Three-state outputs for each counter provide pulses or levels and can be active-high or active-low. The counters can be programmed to count up or down in either binary or BCD. The host processor may read an accumulated count at any time without disturbing the counting process. Any of the counters may be internally concatenated to form any effective counter length up to 80 bits.

The AmZ8073* is functionally equivalent to the Am9513 with timing enhancements which allow it to be fully speed compatible with the AmZ8001 and AmZ8002 microprocessors.

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ORDERING INFORMATION

Package Type	Counting Frequency Temperature Range	7MHz
Molded	$0°C \leq T_A \leq +70°C$	AM9513PC
Hermetic		AM9513DC
Hermetic	$-40°C \leq T_A \leq +85°C$	AM9513DI
Hermetic	$-55°C \leq T_A \leq +125°C$	AM9513DM
Molded	$0°C \leq T_A \leq +70°C$	AMZ8073PC
Hermetic		AMZ8073DC
Hermetic	$-40°C \leq T_A \leq +85°C$	AMZ8073DI

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MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

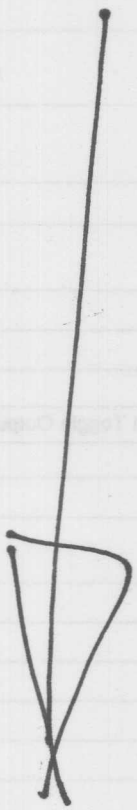
Part Number	Temperature	VCC	VSS
Am9513DC/PC	$0°C \leq T_A \leq +70°C$	+5V ±5%	0V
Am9513DI	$-40°C \leq T_A \leq +85°C$	+5V ±5%	0V
Am9513DM	$-55°C \leq T_A \leq +125°C$	+5V ±5%	0V
AmZ8073DC/PC	$0°C \leq T_A \leq +70°C$	+5V ±5%	0V
AmZ8073DI	$-40°C \leq T_A \leq +85°C$	+5V ±5%	0V

ELECTRICAL CHARACTERISTICS over operating range (Notes 1 and 2)

Parameter	Description		Test Conditions	Min	Typ	Max	Units
VIL	Input Low Voltage	All Inputs Except X2		VSS−0.5		0.8	Volts
		X2 Input		VSS−0.5		0.8	
VIH	Input High Voltage	All Inputs Except X2		2.2V		VCC	Volts
		X2 Input		3.8		VCC	
VITH	Input Hysteresis (SRC and GATE Inputs Only)			0.2	0.3		Volts
VOL	Output Low Voltage		IOL = 3.2mA			0.4	Volts
VOH	Output High Voltage		IOH = −200μA	2.4			Volts
IIX	Input Load Current (Except X2)		$VSS \leq VIN \leq VCC$			±10	μA
IOZ	Output Leakage Current (Except X1)		$VSS + 0.4 \leq VOUT \leq VCC$ High Impedance State			±25	μA
ICC	VCC Supply Current (Steady State)		$T_A = -55°C$			275	mA
			$T_A = 0°C$			255	
			$T_A = +25°C$		190	235	
CIN	Input Capacitance		f = 1MHz, $T_A = +25°C$, All pins not under test at 0V.			10	pF
COUT	Output Capacitance					15	
CIO	IN/OUT Capacitance					20	

SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 4)

Parameter	Description		Figure	Am9513 Min	Am9513 Max	AmZ8073 Min	AmZ8073 Max	Units
TAVRL	C/$\overline{D}$ Valid to Read Low		23	25		25		ns
TAVWH	C/$\overline{D}$ Valid to Write High		23	170		170		ns
TCHCH	X2 High to X2 High (X2 Period)		24	145		145		ns
TCHCL	X2 High to X2 Low (X2 High Pulse Width)		24	70		70		ns
TCLCH	X2 Low to X2 High (X2 Low Pulse Width)		24	70		70		ns
TDVWH	Data In Valid to Write High		23	80		80		ns
TEHEH	Count Source High to Count Source High (Source Cycle Time) (Note 10)		24	145		145		ns
TEHEL TELEH	Count Source Pulse Duration (Note 10)		24	70		70		ns
TEHFV	Count Source High to FOUT Valid (Note 10)		24		500		500	ns
TEHGV	Count Source High to Gate Valid (Level Gating Hold Time) (Notes 10, 12, 13)		24	10		10		ns
TEHRL	Count Source High to Read Low (Set-up Time) (Notes 5, 10)		23	190		190		ns
TEHWH	Count Source High to Write High (Set-up Time) (Notes 6, 10)		23	−100		−100		ns
TEHYV	Count Source High to Out Valid (Note 10)	TC Output	24		300		300	ns
		Immediate or Delayed Toggle Output	24		300		300	
		Comparator Output	24		350		350	
TFN	FN High to FN+1 Valid (Note 14)		24		75		75	ns
TGVEH	Gate Valid to Count Source High (Level Gating Set-up Time) (Notes 10, 12, 13)		24	100		100		ns
TGVGV	Gate Valid to Gate Valid (Gate Pulse Duration) (Notes 11, 13)		24	145		145		ns
TGVWH	Gate Valid to Write High (Notes 6, 13)		23	−100		−100		ns
TRHAX	Read High to C/$\overline{D}$ Don't Care		23	0		0		ns
TRHEH	Read High to Count Source High (Notes 7, 10)		23	0		0		ns
TRHQX	Read High to Data Out Invalid		23	10		10		ns
TRHQZ	Read High to Data Out at High Impedance (Data Bus Release Time)		23		85		85	ns
TRHRL	Read High to Read Low (Read Recovery Time)		23	1000		1000		ns
TRHSH	Read High to $\overline{CS}$ High (Note 15)		23	0		0		ns
TRHWL	Read High to Write Low (Read Recovery Time)		23	1000		1000		ns
TRLQV	Read Low to Data Out Valid		23		110		110	ns
TRLQX	Read Low to Data Bus Driven (Data Bus Drive Time)		23	20		20		ns
TRLRH	Read Low to Read High (Read Pulse Duration) (Note 15)		23	160		160		ns
TSLRL	$\overline{CS}$ Low to Read Low (Note 15)		23	20		20		ns
TSLWH	$\overline{CS}$ Low to Write High (Note 15)		23	170		170		ns
TWHAX	Write High to C/$\overline{D}$ Don't Care		23	20		20		ns
TWHDX	Write High to Data In Don't Care		23	20		20		ns
TWHEH	Write High to Count Source High (Notes 8, 10, 17)		23	550		550		ns
TWHGV	Write High to Gate Valid (Notes 8, 13, 17)		23	500		500		ns
TWHRL	Write High to Read Low (Write Recovery Time)		23	1500		1000		ns
TWHSH	Write High to $\overline{CS}$ High (Note 15)		23	20		20		ns
TWHWL	Write High to Write Low (Write Recovery Time)		23	1500		1000		ns
TWHYV	Write High to Out Valid (Note 9, 17)		23		650		650	ns
TWLWH	Write Low to Write High (Write Pulse Duration) (Note 15)		23	150		150		ns



The International Standard of Quality guarantees these electrical AQLs on all parameters over the operating temperature range: 0.1% on MOS RAMs & ROMs; 0.2% on Bipolar Logic & Interface; 0.3% on Linear, LSI, Logic & other memories.

INT-STD-121

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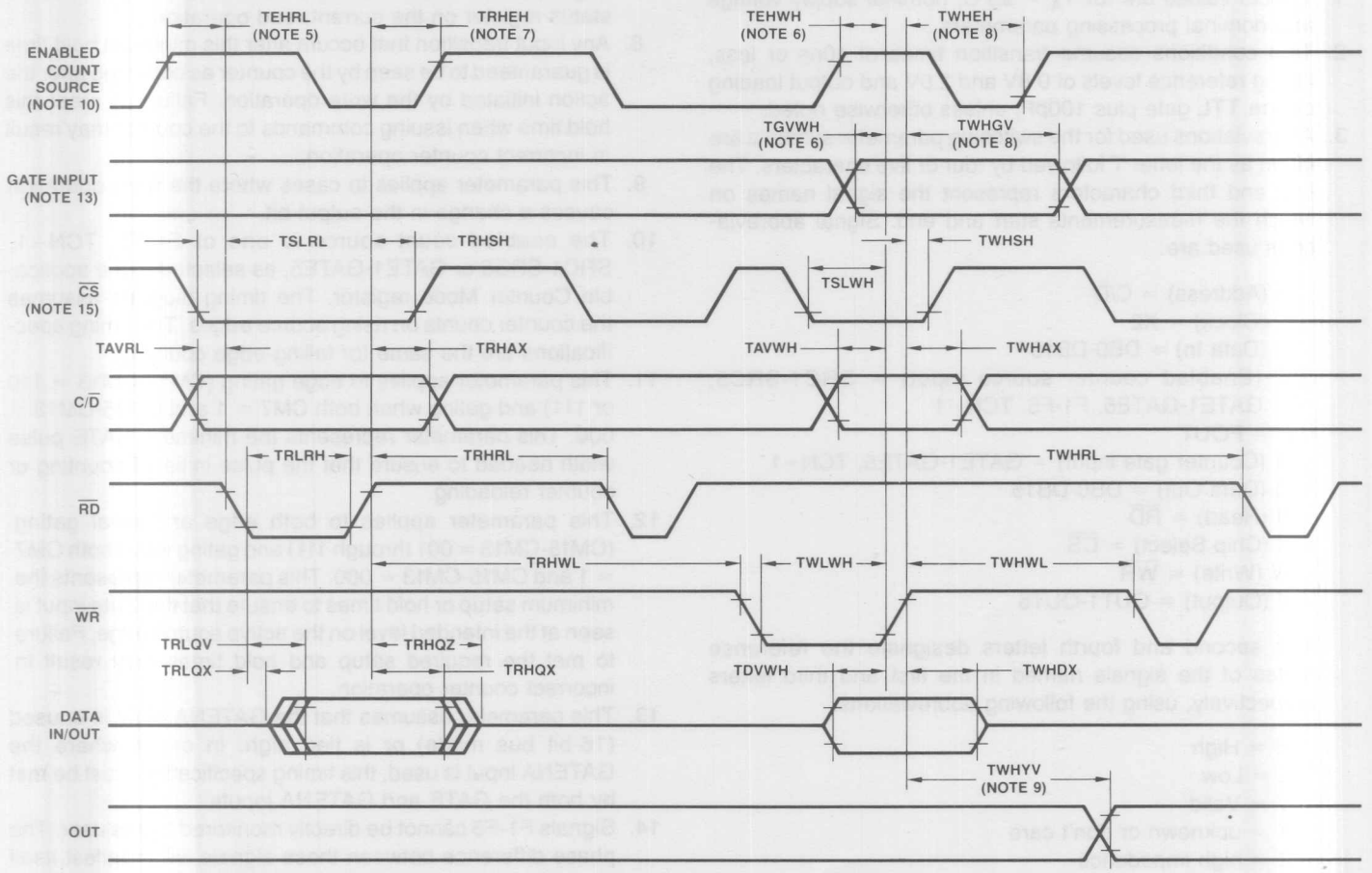
Bus Transfer Switching Waveforms



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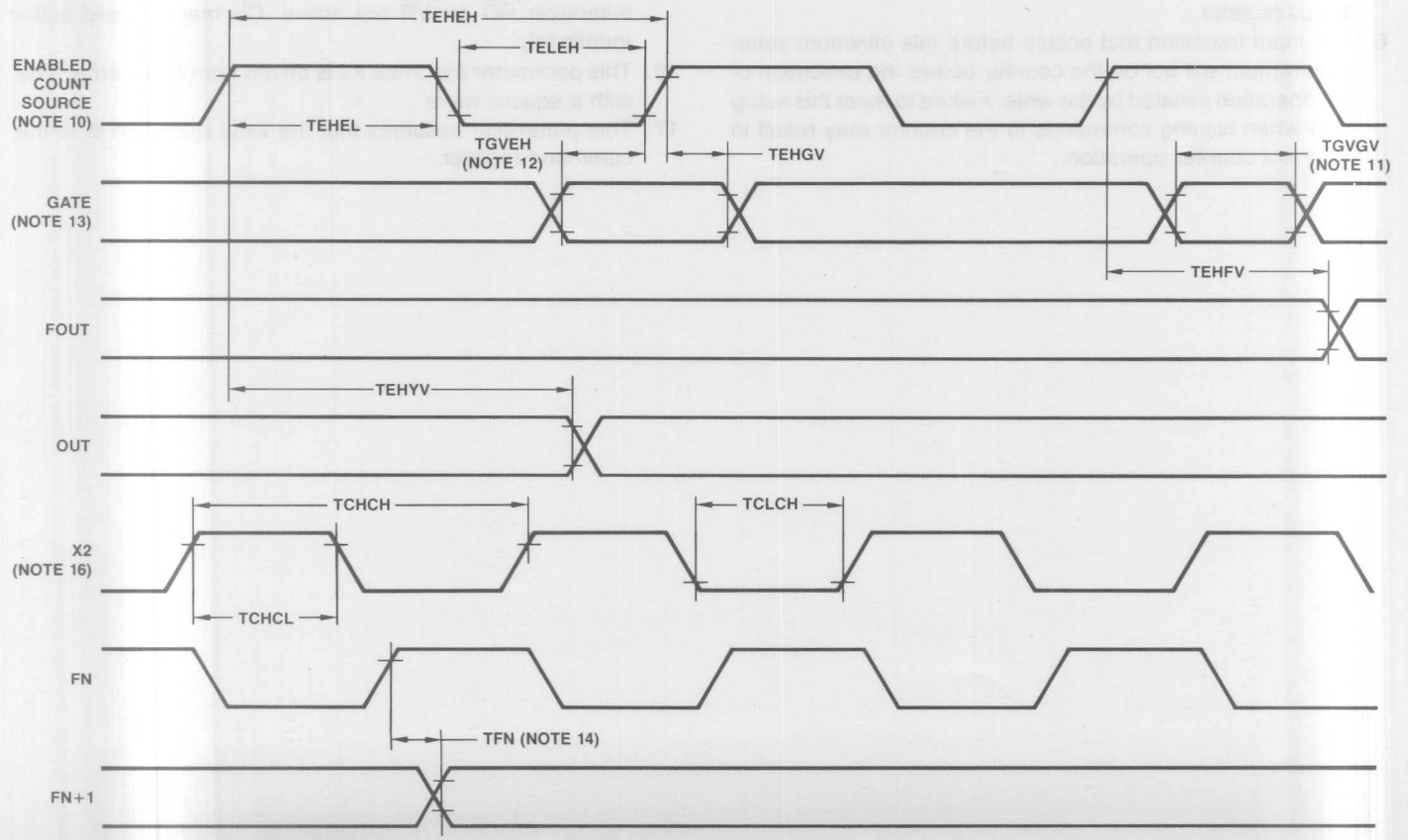
Counter Switching Waveforms



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NOTES:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Test conditions assume transition times of 10ns or less, timing reference levels of 0.8V and 2.0V and output loading of one TTL gate plus 100pF, unless otherwise noted.
3. Abbreviations used for the switching parameter symbols are given as the letter T followed by four or five characters. The first and third characters represent the signal names on which the measurements start and end. Signal abbreviations used are:

   A (Address) = C/$\overline{D}$
   C (Clock) = X2
   D (Data In) = DB0-DB15
   E (Enabled counter source input) = SRC1-SRC5, GATE1-GATE5, F1-F5, TCN−1
   F = FOUT
   G (Counter gate input) = GATE1-GATE5, TCN−1
   Q (Data Out) = DB0-DB15
   R (Read) = $\overline{RD}$
   S (Chip Select) = $\overline{CS}$
   W (Write) = $\overline{WR}$
   Y (Output) = OUT1-OUT5

   The second and fourth letters designate the reference states of the signals named in the first and third letters respectively, using the following abbreviations.

   H = High
   L = Low
   V = Valid
   X = unknown or don't care
   Z = high impedance

4. Switching parameters are listed in alphabetical order.
5. Any input transition that occurs before this minimum setup requirement will be reflected in the contents read from the status register.
6. Any input transition that occurs before this minimum setup requirement will act on the counter before the execution of the operation initiated by the write. Failure to meet this setup time when issuing commands to the counter may result in incorrect counter operation.
7. Any input transition that occurs after this minimum hold time is guaranteed to not influence the contents read from the status register on the current read operation.
8. Any input transition that occurs after this minimum hold time is guaranteed to be seen by the counter as occurring after the action initiated by the write operation. Failure to meet this hold time when issuing commands to the counter may result in incorrect counter operation.
9. This parameter applies to cases where the write operation causes a change in the output bit.
10. The enabled count source is one of F1-F5, TCN−1, SRC1-SRC5 or GATE1-GATE5, as selected in the applicable Counter Mode register. The timing diagram assumes the counter counts on rising source edges. The timing specifications are the same for falling-edge counting.
11. This parameter applies to edge gating (CM15-CM13 = 110 or 111) and gating when both CM7 = 1 and CM15-CM13 ≠ 000. This parameter represents the minimum GATE pulse width needed to ensure that the pulse initiates counting or counter reloading.
12. This parameter applies to both edge and level gating (CM15-CM13 = 001 through 111) and gating when both CM7 = 1 and CM15-CM13 = 000. This parameter represents the minimum setup or hold times to ensure that the Gate input is seen at the intended level on the active source edge. Failure to met the required setup and hold times may result in incorrect counter operation.
13. This parameter assumes that the GATENA input is unused (16-bit bus mode) or is tied high. In cases where the GATENA input is used, this timing specification must be met by both the GATE and GATENA inputs.
14. Signals F1-F5 cannot be directly monitored by the user. The phase difference between these signals will manifest itself by causing counters using two different F signals to count at different times on nominally simultaneous transitions in the F signals.
15. This timing specification assumes that $\overline{CS}$ is active whenever $\overline{RD}$ or $\overline{WR}$ are active. $\overline{CS}$ may be held active indefinitely.
16. This parameter assumes X2 is driven from an external gate with a square wave.
17. This parameter assumes that the write operation is to the command register.